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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,527	03/24/2004	Hei Ming Shiu	SC13154HP	3435

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EXAMINER	
TRAN, THANH Y	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/807,527	HEI MING SHIU	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/17/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Igarashi et al (U.S. 2004/0097081) in view of Kitahara (U.S. 5,568,363).

As to claims 1-4, 6 and 12-14, Igarashi discloses in figures 1-14 an apparatus and a corresponding method of packaging an integrated circuit die (comprising elements 19, 11A), comprising the steps of: providing a sheet ("substrate"12); forming a single layer of solder ("conductive film" 13) on a first side of the sheet (12); attaching a first side of an integrated circuit die (19, 11A) to the single solder layer (13) on the sheet (12), wherein the first side of the die (19, 11A) includes a layer of metal (14A) thereon and a second, opposing side of the die includes a plurality of bonding pads (see pads on surface of element 19); electrically connecting the bonding pads (14A) to the single solder layer (13), via pattern 11A, on the sheet (12) with a plurality of wires (see wires in figures 9-14); encapsulating the die (comprising elements 19, 11A), the electrical connections (including conductive elements wires, pads 14), and the first side of the sheet (12) with a mold compound (22); and separating the sheet (12) from the die (see figures 10-11) and the plurality of wires, thereby forming a packaged integrated circuit (as shown in figures 11-14); wherein the solder (13) is formed on the sheet (12) via a screen printing

process (see [0094]); performing a first reflow process [*a first reflow process is the melting process of solder layer 13 to secure die (19, 11A) to the sheet 12*] after the die attach step (see figures 1-9), wherein the first reflow process to melts the solder (13), thereby securing the die (*19, 11A*) to the sheet (12); wherein the sheet (12) is separated from the die (comprising elements 19, 11A) (figures 10-11) and the wires via a second reflow process; wherein a portion of the solder (13) remains attached to the wires (figure 11) and the die (comprising elements 19, 11A) after the sheet (12) is separated therefrom; wherein the more than one die (see figures 9-14) is attached to the sheet (12), and after the sheet (12) is separated from the die (comprising 19, 11A) and the wires (figures 10-14), the die (comprising 19, 11A) and the wires connected to the respective die are separated from each other such that multiple packaged devices are formed substantially simultaneously (see figures 12 and 14).

Igarashi does not disclose the sheet is a foil sheet; wherein the foil sheet comprises a bare metal sheet; wherein the metal sheet comprises copper.

Kitahara discloses in figures 1-2 an apparatus and a method comprising a die (120) attached to the foil sheet ("lead" 3); where the foil sheet (3) comprises a bare metal sheet (conductive sheet); wherein the metal sheet comprises copper (col. 1, lines 45-50). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Igarashi by replacing a sheet with a foil sheet as taught by Kitahara for supporting the chip during the process steps.

As to claim 8, Igarashi discloses in figures 1-14 an apparatus and a corresponding method of packaging an integrated circuit die (comprising elements 19, 11A), wherein the plurality of

wires (as shown in figures 9-14) are attached to the bonding pads (14A) and the solder (13) via a wire bonding process.

As to claim 9, Igarashi discloses in figures 1-14 an apparatus and a corresponding method of packaging an integrated circuit die (comprising elements 19, 11A), wherein the wirebonding process comprises a ball bonding process (see balls 24, figures 13-14).

As to claims 5, 10-11 and 16, Igarashi does not disclose the solder layer has a thickness of about 0.1 mm; squashed ball bonds of the bonding process that inherently function as package terminals has a diameter of about 0.25 mm; or the wires have a diameter of about 50 um to about 100 um. However, the thickness of solder layer; or the diameter of squashed ball bonds or wires would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 15, Igarashi discloses in figures 1-14 an apparatus and a corresponding method of forming a plurality of integrated circuit packages, comprising the steps of: providing a sheet (12); forming a layer of high temperature solder (13) on a first side of the sheet (12) via a screen printing process (see [0094]); attaching first sides of a plurality of integrated circuit dies (each die comprising elements 19, 11A) to the single solder layer (13) on the sheet (12), wherein

the first side of each of the die (19, 11A) includes a layer of metal (14A) thereon and a second, opposing side of each of the die includes a plurality of bonding pads (see pads on surface of element 19); performing a first reflow process for securing the plurality of integrated circuit dies (each die comprising elements 19, 11A) to the sheet (12); electrically connecting the bonding pads (see pads on surface of element 19) to the single solder layer (13) on the sheet (12) with a plurality of wires via a wirebonding process (comprising elements 14A, 11A and 13), wherein first ends of the wires (see figures 9-14) are attached to the bonding pads (see pads on surface of element 19) and second ends of the wires are attached to the sheet (12); encapsulating the integrated circuit dies (see element 22), the electrical connections (including 11A, 14A and wires), and the first side of the sheet (12) with a mold compound (22); separating the sheet (12) and the solder layer (13) from the integrated circuit dies (comprising elements 19, 11A), second ends of the plurality of wires (see figures 12 and 14), and the mold compound (22) via a second reflow process, wherein only a portion of the solder layer (13) is removed from the dies and the second ends of the plurality of wires; and separating the encapsulated integrated circuit dies (each die comprising elements 19, 11A) and the wires connected thereto from other ones of the encapsulated integrated circuit dies, thereby forming a plurality of packaged integrated circuits (as shown in figures 12 and 14).

Igarashi does not the sheet is a metal foil. Kitahara discloses in figures 1-2 and apparatus and a method comprising a die (120) attached to the metal foil ("foil lead" 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Igarashi by having replacing a sheet with a foil sheet as taught by Kitahara for supporting the chip during the process steps.

As to claims 17 and 19, Igarashi discloses in figures 1-14 an apparatus and a corresponding method of forming a plurality of integrated circuit packages, wherein the separating step comprises the step of saw singulating the encapsulated die (comprising elements 19, 11A) from adjacent encapsulated dies (see figures 12 and 14).

As to claims 18 and 20, Igarashi discloses in figures 1-14 an apparatus and a corresponding method of forming a multi-chip module, comprising the steps of: providing a sheet (12); forming a single layer of high temperature solder (13) on a first side of the sheet (12) via a screen printing process (see [0094]); attaching first sides of at least two integrated circuit dies (each die comprising elements 19 and 11A) to the single solder layer (13) on the sheet (12), wherein the first side of each of the die (19, 11A) includes a layer of metal (14A) thereon and a second, opposing side of each of the die (19, 11A) includes a plurality of bonding pads (see pads on surface of element 19); performing a first reflow process for securing the at least two integrated circuit dies (each die comprising elements 19 and 11A) to the sheet (12); electrically connecting a first portion of the bonding pads (see pads on surface of element 19) of each of the at least two dies to the single solder layer (13) on the sheet (12) with a plurality of first wires (see wires in figures 9-14) via a first wirebonding process (including pads 14A and wires), wherein first ends of the first wires are attached to the bonding pads (see pads on surface of element 19) and second ends of the first wires are attached to the sheet (12) (via elements 14A, 11A); electrically connecting the at least two dies to each other by connecting a second portion of the bonding pads (see second portion pads on surface of element 19) of a first one of the die (19, 11A) to a second portion of the bonding pads of a second one of the dies (see second die 19, 11A) with a plurality of second wires via a second wirebonding process (see second pads 14A

and wires); encapsulating the at least two integrated circuit dies (each die comprising elements 19 and 11A), the electrical connections (such as pads 14A and wires), and the first side of the sheet (12) with a mold compound (22); and separating the sheet (12) and the solder layer (13) from the at least two integrated circuit dies (each die comprising elements 19 and 11A), second ends of the plurality of first wires (see first wires of each die), and the mold compound (22) via a second reflow process, wherein only a portion of the solder layer (13) is removed from the at least two dies (each die comprising elements 19 and 11A) and the second ends of the plurality of wires (see second end of the plurality of wires of each die); attaching a passive device (a separate smaller portion 11A can be a passive device) to the solder (13) on the sheet (12); and electrically connecting the passive device to at least one of the at least two dies, and wherein the passive device is encapsulated with the mold compound (22) (figs. 10-14).

Igarashi does not the sheet is a metal foil. Kitahara discloses in figures 1-2 and apparatus and a method comprising a die (120) attached to the metal foil ("foil lead" 3). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Igarashi by having replacing a sheet with a foil sheet as taught by Kitahara for supporting the chip during the process steps.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 6, 10, 15-16, and 18 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argued that Kitahara does not use any wire bonding processes, nor form any ball bonds.

In response, the examiner agrees with applicant's argument that Kitahara does not use any wire bonding processes, nor form any ball bonds because Kitahara only teaches a method comprising: a sheet foil sheet 3 comprises a bare metal sheet (conductive sheet), and wherein the metal sheet comprises copper (col.. 1, lines 45-50) (see the above rejected claim 1).

Applicant further argued that the copper sheet of Kitahara cannot be properly combined with the process taught by Igarashi because Kitahara is a lead frame type process.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Igarashi et al (U.S. 2004/0097081) discloses all limitations (as recited in claim 1), except for a foil sheet that comprises a bare metal sheet, wherein the metal sheet comprises copper. However, Kitahara discloses in figures 1-2 an apparatus and a method comprising: a foil sheet (3) comprises a bare metal sheet (conductive sheet); wherein the metal sheet comprises copper (col. 1, lines 45-50). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Igarashi by replacing a layer of Igarashi with a foil sheet as taught by Kitahara for supporting the chip during the process steps.

Applicant further argued that the lead frame of Kitahara would not be removable.

In response, the examiner does not agree with applicant's argument because applicant argued the limitation that is not recited in the claim.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
30 May 2006